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EXAMINER	
TANG, KENNETH	

ART UNIT	PAPER NUMBER
2195	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/621,067	FARKAS ET AL.	
	Examiner	Art Unit	
	KENNETH TANG	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,8,15,17-27 and 29-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,8,15,17-27 and 29-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 7-8, 15, and 17-27, and 29-36 are presented for examination.

2. This action is in response to the Amendment on 4/23/09. Applicant's arguments have been fully considered but are moot in view of the new grounds of rejections.

3. The indicated allowability of claims 20, 21, and 29 are withdrawn in view of the newly discovered reference(s) to Kumar et al. (hereinafter Kumar) ("Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures", IEEE Computer Architecture Letters, Vol. 2, April 2003). Rejections based on the newly cited reference(s) follow.

Claim Objections

4. Claim 27 is objected to because of the following informalities: Dependent claims must depend upon preceding claims. Therefore, it is improper for claim 27 to depend on claim 29. Appropriate correction is required.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting

ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents).

7. Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 7,093,147 B2 in view of Kumar et al. (hereinafter Kumar) ("Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures", IEEE Computer Architecture Letters, Vol. 2, April 2003).

8. As to claim 1, U.S. Patent No. 7,093,147 B2 teaches a computer system, comprising:

a plurality of computer processor cores in which at least two of the computer processor cores are heterogeneous, and wherein the plurality of computer processor cores all execute the same instruction set (col. 8, lines 50-53); and

a performance measurement (col. 8, lines 61-63) and transfer mechanism configured to move a plurality of computer processing jobs amongst the plurality of computer processor cores (col. 8, lines 64-67).

9. U.S. Patent No. 7,093,147 B2 is silent in matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor core.

10. However, Kumar teaches matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor core (evaluates the resource requirements of an application and chooses the core that can best meet these requirements) (see Title and Abstract; page 1, 2nd paragraph under the "I. INTRODUCTION" section; page 1, under section "II. Architecture"). One of ordinary skill in the art would have known to modify U.S. Patent No. 7,093,147 B2 such that it would include the feature of matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor core, as taught in Kumar. The suggestion/motivation for doing so would have been to provide the predicted result of being able to dynamically choose the most appropriate core to meet specific performance and power requirements (see Abstract). Therefore, it would have been obvious to one of ordinary skill in the art to combine claim 1 of U.S. Patent No. 7,093,147 B2 and Kumar to obtain the invention of claim 1.

11. Claim 7 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 7,093,147 B2 in view of Kumar et al. (hereinafter Kumar) ("Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures", IEEE Computer Architecture Letters, Vol. 2, April 2003).

12. As to claim 7, U.S. Patent No. 7,093,147 B2 teaches a method for operating multiple processor cores, comprising:

placing a plurality of computer processor cores on a single semiconductor die, in which at least two computer processor cores differ in processing performance, and in which all execute the same instruction set (col. 10, lines 39-46);

measuring the performance of each of a plurality of computer processing jobs hosted amongst the plurality of computer processor cores (col. 10, lines 49-51); and

transferring individual ones of said plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores to improve a throughput metric (col. 10, lines 52-55).

13. U.S. Patent No. 7,093,147 B2 is explicitly silent in obtaining a throughput metric that identifies throughput achieved by the computer processor cores as a function of workloads running on said computer processor cores.

14. However, Kumar teaches a method for operating multiple processor cores, comprising: obtaining a throughput metric that identifies throughput achieved by a plurality of computer processor cores as a function of workloads running on said computer processor cores, wherein the plurality of computer processor cores are on a single semiconductor die, in which at least two computer processor cores differ in processing capability, and wherein the computer processor cores execute the same instruction set (heterogeneous set of cores on a single multi-core die, sharing the same ISA. To do this, we constrain the problem to a single application switching among cores to optimize some function of energy and performance) (page 4, 1st paragraph under

Section VI. "CONCLUSIONS AND FUTURE WORK"; see Title and Abstract; page 1, 2nd paragraph under the "I. INTRODUCTION" section); and transferring individual ones of a plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores to improve a throughput metric (for a particular performance/throughput requirement or goal) (page 1, under Section II: "ARCHITECTURE"; page 4, 3rd paragraph of Section V: "RELATED WORK").

15. One of ordinary skill in the art would have known to modify U.S. Patent No. 7,093,147 B2 such that it would include the feature of obtaining a throughput metric that identifies throughput achieved by the computer processor cores as a function of workloads running on said computer processor cores, as taught in Kumar. The suggestion/motivation for doing so would have been to provide the predicted result of being able to dynamically choose the most appropriate core to meet specific performance and power requirements (see Abstract). Therefore, it would have been obvious to one of ordinary skill in the art to combine claim 14 of U.S. Patent No. 7,093,147 B2 and Kumar to obtain the invention of claim 7.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

16. Claims 1-2, 7-8, 15, 17-22, 24-27, and 29-36 are rejected under 35 U.S.C. 102(a) as being anticipated by Kumar et al. (hereinafter Kumar) ("Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures", IEEE Computer Architecture Letters, Vol. 2, April 2003).

17. As to claim 1, Kumar teaches a computer system (computer system with Single-ISA Heterogeneous Multi-Core Architectures) (see Title and Abstract), comprising:

a plurality of computer processor cores in which at least two differ of the computer processor cores are heterogeneous, and wherein the plurality of computer processor cores execute the same instruction set (computer system with Single-ISA Heterogeneous Multi-Core Architectures) (see Title and Abstract; page 1, 2nd paragraph under the "I. INTRODUCTION" section); and

a performance measurement and transfer mechanism configured to move a plurality of executing computer processing jobs amongst the plurality of computer processor cores by matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor cores (evaluates the resource requirements of an application and chooses the core that can best meet these requirements) (see Title and Abstract; page 1, 2nd paragraph under the "I. INTRODUCTION" section).

18. As to claim 2, Kumar teaches further comprising: at least one of an operating system, hosted on the plurality of computer processor cores, firmware, and special-purpose hardware that

includes the performance measurement and transfer mechanism, and the at least one of the operating system, firmware, and special-purpose hardware is configured to provide for a periodic (performed dynamically) test to determine relative performance of different jobs on different ones of the plurality of computer processor cores (see Abstract; page 1, under section "II. Architecture").

19. As to claim 7, Kumar teaches a method for operating multiple processor cores, comprising:

obtaining a throughput metric that identifies throughput achieved by a plurality of computer processor cores as a function of workloads running on said computer processor cores, wherein the plurality of computer processor cores are on a single semiconductor die, in which at least two computer processor cores differ in processing capability, and wherein the computer processor cores execute the same instruction set (heterogeneous set of cores on a single multi-core die, sharing the same ISA. To do this, we constrain the problem to a single application switching among cores to optimize some function of energy and performance) (page 4, 1st paragraph under Section VI. "CONCLUSIONS AND FUTURE WORK"; see Title and Abstract; page 1, 2nd paragraph under the "I. INTRODUCTION" section); and

transferring individual ones of a plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores to improve a throughput metric (for a particular performance/throughput requirement or goal) (page 1, under Section II: "ARCHITECTURE"; page 4, 3rd paragraph of Section V: "RELATED WORK").

20. As to claim 8, Kumar teaches providing for a periodic test to determine relative performance of different jobs on different ones of the computer processor cores (dynamically chooses the most appropriate core to meet specific performance/throughput and power requirements) (see Abstract).

21. As to claim 15, Kumar teaches further comprising: associating workloads for execution on specific processor cores based on annotations (application job requirements, etc.) associated with the computer processing jobs (page 1, 2nd paragraph under the "I. INTRODUCTION" section, Abstract).

22. As to claim 17, Kumar teaches further comprising at least one of an operating system hosted on the plurality of computer processor cores, firmware, and special-purpose hardware that includes the performance measurement and transfer mechanism (see Abstract; page 1, under section "II. Architecture").

23. As to claim 18, Kumar teaches wherein the performance measurement and transfer mechanism is configured to maximize total system throughput (optimize some function of energy and performance/throughput) (page 4, under "Section VI: CONCLUSIONS AND FUTURE WORK"; and page 4, 1st column, 1st paragraph, last two sentences).

24. As to claim 19, Kumar teaches wherein the performance measurement and transfer mechanism is configured to transfer the executing computer processing jobs to a new assignment amongst the plurality of computer processor cores, collect performance statistics about execution at the new assignment, and then determine whether to reassign the executing computer processing jobs to different computer processor cores based on the performance statistics collected (dynamically evaluates the resource requirements of an application and chooses the core that can best meet these requirements) (see Title and Abstract; page 1, 2nd paragraph under the "I. INTRODUCTION" section; see Fig. 2).

25. As to claim 20, Kumar teaches a computer system (computer system with Single-ISA Heterogeneous Multi-Core Architectures) (see Title and Abstract), comprising:

a plurality of computer processor cores in which at least two differ in processing performance, and wherein the plurality of computer processor cores execute the same instruction set (computer system with Single-ISA Heterogeneous Multi-Core Architectures) (see Title and Abstract; page 1, 2nd paragraph under the "I. INTRODUCTION" section); and

a performance measurement and transfer mechanism configured to move a plurality of executing computer processing jobs amongst the plurality of computer processor cores based on a measured throughput metric (matches the applications to the different cores based on a given performance/throughput requirement or goal) (see Abstract; page 1, under section "II. Architecture"),

wherein the performance and transfer mechanism is configured to swap execution (core-switching approach) of the executing computer processing jobs between the computer processor cores for a period of time (during execution, etc.), monitor resulting performance, and then build a data structure with relative performances of jobs on different types of computer processor cores (page 3, Section "D. Modeling Performance"; Abstract; page 1, under section "II Architecture").

26. As to claim 21, Kumar teaches wherein the jobs are reassigned based on the relative performances, by assigning jobs that benefited most from large complex cores to said large complex cores (reassigning/switching based on relative performances of complexity/performance continuum) (page 3, TABLE I, and 1st column, 2nd paragraph; page 1, under section "II Architecture").

27. As to claim 22, Kumar teaches wherein the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics (page 1, 3rd paragraph of Section "I: INTRODUCTION").

28. As to claim 24, Kumar teaches wherein movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals (switch only at operating system timeslice intervals) (page 2, 2nd column, 2nd sentence of 2nd paragraph).

29. As to claim 25, Kumar teaches a method for operating multiple processor cores, comprising:

assigning a plurality of computer processing jobs amongst a plurality of computer processor cores, wherein at least two of the computer processor cores differ in size and complexity but execute the same instruction set (computer system with Single-ISA Heterogeneous Multi-Core Architectures that reassigns/switches based on relative performances of complexity/performance continuum) (page 3, TABLE I, and 1st column, 2nd paragraph; page 1, under section "II Architecture"), and

wherein assigning the plurality of computer processing jobs amongst the plurality of computer processor cores comprises matching requirements of the computer processing jobs to processing capabilities of the computer processor cores based on the sizes or complexities of the computer processor cores (These cores all execute the same instruction set, but include significantly different resources, and achieve different performance and energy efficiency on the same application. During execution, the operating system matches the applications to the different cores based on a given performance/throughput requirement or goal) (see Abstract; page 1, under section "II. Architecture").

30. As to claim 26, it is rejected for the same reasons as stated in the rejection of claim 8.

31. As to claim 27, it is rejected for the same reasons as stated in the rejection of claim 18.

32. As to claim 29, Kumar teaches a method for operating multiple processor cores, comprising:

obtaining a throughput metric that identifies throughput achieved by computer processor cores on a single semiconductor die as a function of workloads running on said computer processor cores (heterogeneous set of cores on a single multi-core die, sharing the same ISA. To do this, we constrain the problem to a single application switching among cores to optimize some function of energy and performance) (page 4, 1st paragraph under Section VI. "CONCLUSIONS AND FUTURE WORK"; see Title and Abstract; page 1, 2nd paragraph under the "I. INTRODUCTION" section); and

assigning a plurality of computer processing jobs amongst a plurality of computer processor cores based on the throughput metric, wherein at least two of the computer processor cores differ in size or complexity but execute the same instruction set (computer system with Single-ISA Heterogeneous Multi-Core Architectures that reassigns/switches based on relative performances of complexity/performance continuum) (page 3, TABLE I, and 1st column, 2nd paragraph; page 1, under section "II Architecture");

transferring the computer processing jobs to a new assignment amongst the plurality of computer processor cores (for a particular performance/throughput requirement or goal) (page 1, under Section II: "ARCHITECTURE"; page 4, 3rd paragraph of Section V: "RELATED WORK");

collecting statistics about execution performance of the computer processing jobs at the new assignment (dynamically evaluates the resource requirements of an application and chooses

the core that can best meet these requirements) (see Title and Abstract; page 1, 2nd paragraph under the "I. INTRODUCTION" section; see Fig. 2);

determining whether to reassign the computer processing jobs to different computer processor cores based on the statistics collected (dynamically evaluates the resource requirements of an application and chooses the core that can best meet these requirements) (see Title and Abstract; page 1, 2nd paragraph under the "I. INTRODUCTION" section; see Fig. 2); and

building a data structure with relative performances of the computer processing jobs on different types of computer processor cores based on statistics collected (page 3, Section "D. Modeling Performance"; Abstract; page 1, under section "II Architecture").

33. As to claims 30-31, they are rejected for the same reasons as stated in the rejections of claims 22-23, respectively.

34. As to claim 32, Kumar teaches wherein the processing capabilities of the computer processor cores are defined by one or more of chip area, available resource, and relative speed of the computer processor cores (page 3, Sections "C. Estimating Chip area" and "D. Modeling Performance"; Table II).

35. As to claim 33, it is rejected for the same reasons as stated in the rejection of claim 15.

36. As to claim 34, Kumar teaches wherein the performance measurement and transfer mechanism is configured to further re-assign the plurality of executing computer processing jobs amongst the plurality of computer processor cores by repeatedly performing a test to match the requirements of the plurality of executing computer processing jobs to the processing capabilities of the computer processor cores (dynamically chooses the most appropriate core to meet specific performance/throughput and power requirements) (see Abstract, page 1, under section "II Architecture").

37. As to claim 35, it is rejected for the same reasons as stated in the rejection of claim 15.

38. As to claim 36, Kumar teaches repeatedly performing a test to match requirements of the computer processing jobs to the processing capabilities of the computer processor cores; and reassigning the plurality of computer processing jobs amongst the plurality of computer processor cores based on the repeated tests (dynamically chooses the most appropriate core to meet specific performance/throughput and power requirements) (see Abstract, page 1, under section "II Architecture").

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. (hereinafter Kumar) ("Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures", IEEE Computer Architecture Letters, Vol. 2, April 2003) in view of Nagae (US 6,006,248).

40. As to claim 23, Kumar is silent in teaching wherein the performance/throughput metric comprises a number of instructions per second. However, Nagae teaches a job application distribution system among a plurality of processors, wherein CPU performance is evaluated and may comprise of the number of instructions per second (col. 18, lines 35-43). One of ordinary skill in the art would have known to modify Kumar's performance/throughput metric such that it would comprise of the number of instructions per second because it would provide the predicted result of utilizing a standard and well-known unit that is common to the user. Therefore, it would have been obvious to combine the references of Kumar and Nagae to obtain the invention of claim 23.

Response to Arguments

41. Applicant's arguments have been fully considered but are now moot in view of the new grounds of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- **Kumar et al. ("Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures", IEEE Computer Architecture Letters, Volume 1, Issue 1, January 2002)** teaches a single-ISA heterogeneous multi-core architecture with a software system that dynamically chooses the most appropriate cores to meet specific performance and power requirements (see Abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH TANG whose telephone number is (571)272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VAN H NGUYEN/
Primary Examiner, Art Unit 2194